InnoDisk FiD ATA4000

Flash in Disk ATA4000

Datasheet

Rev. 1.1

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REVISION HISTORY

Revision	Description	Date
1.0	Release	January 2006
1.1	Modify shock information	

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1. Product Overview

1.1 Introduction to Flash in Disk

Flash in Disk (FiD) ATA4000 products provide high capacity 2.5-inch solid-state flash disk that electrically complies with ATA4 standard. InnoDisk Flash in Disk (FiD) ATA4000 is 2.5-inch solid-state data storage systems for industrial work place.

Flash in Disk (FiD) ATA4000 supports advanced PIO(0-4), Multiword DMA(0-2) and Ultra DMA(0-4) transfer modes, multi-sector transfers, and LBA addressing.

1.2 Product Models

Flash in Disk (FiD) ATA4000 is available in capacities ranging from 4GB to 32GB, , making the upgrade path simple and fast.

1.3 Pin Assignments

FiD ATA4000 uses a standard IDE 44-pin. See Figure 1 & Table 1 for FiD ATA4000 pin assignments.

Figure 1: FiD ATA4000 Connector Layout

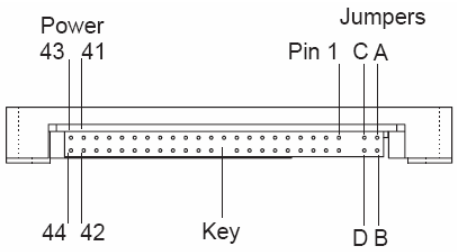


Table 1: FiD ATA4000 Pin Assignment

Pin No.	Name	Function	Pin No.	Name	Function
1	HRESET	Host Reset	2	GND	Ground
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11
11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15
19	GND	Ground	20	KEY	Key-pin
21	DMARQ	DMA Request	22	GND	Ground
23	HIOW[1]	Host I/O Write	24	GND	Ground
	STOP[2]	Stop Ultra DMA burst			
25	HIOR[1]	Host I/O Read	26	GND	Ground
	HDMARDY[2]	Ultra DMA ready			
	HSTROBE[2]	Ultra DMA data strobe			

Pin No.	Name	Function	Pin No.	Name	Function
27	IORDY[1]	I/O Ready	28	CSEL	Master/Slave Select
	DDMARDY[2]	Ultra DMA ready			
	DSTROBE[2]	Ultra DMA data strobe			
29	DMACK	DMA Acknowledge	30	GND	Ground
31	INTRQ	Interrupt Request	32	IOCS16	CS I/O 16-Bit
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic
35	HAB[0]	Host Address Bit 0	36	HAB[2]	Host Address Bit 2
37	CS0	Chip Select 0	38	CS1	Chip Select 1
39	DASP	Drive Active	40	GND	Ground
41	VCC	Supply Voltage	42	VCC	Supply Voltage
43	GND	Ground	44	NC	Not Connected
A	N/A	Master/Slave	B	N/A	Master/Slave
C	N/A	NC	D	N/A	NC

Note:

1. Signal usage in PIO & Multiword DMA mode.
2. Signal usage in Ultra DMA mode.

1.4 Pin Descriptions

Table 2 describes the pin descriptions for FiD ATA4000

Table 2: FiD ATA4000 Pin Descriptions

Pin Name	Pin No.	Description	I/O
Host side pins			
HRESET-	1	Host reset signal, High: Reset.	I
CS0-	37	Chip select CS0	I
CS1-	38	Chip select CS1	I
INTRQ	31	Host interrupt signal.	O
HIOR-[1]	25	I/O read strobe signal.	I
HDMARDY-[2]		DMA ready during Ultra DMA data in burst	
HSTROBE[2]		Data strobe during Ultra DMA data out burst	
HIOW-[1]	23	I/O write strobe signal.	I
STOP[2]		Stop during Ultra DMA data bursts	
IOCS16-	32	Asserted in 16-bit access.	O
IORDY[1]	27	I/O Ready Signal	O
DDMARDY-[2]		DMA ready during Ultra DMA data out burst	
DSTROBE[2]		Data strobe during Ultra DMA data in burst	
HDB[15:0]	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	Host data bus	I/O
HAB[2:0]	33, 35, 36	Host Address bus	I/O
CSEL-	28	Master/Slave select signal (cable select signal). Low: Device operates as a master, High: Device operates as a slave.	I
DASP-	39	Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.	I/O
PDIAG-	34	Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.	I/O
DMARQ	21	DMA Request.	O
DMACK-	29	DMA Acknowledge.	I

Pin Name	Pin No.	Description	I/O
Power and Ground			
VCC	41, 42	Connect to VCC	VCC
GND	2, 19, 22, 24, 26, 30, 40, 43	Connect to GND.	GND
Other pins			
KEY	20	Key-Pin	N/A
Master/Slave	A, B	Master/Slave	N/A
NC	44, C, D	Not used. Please do not connect.	N/A

Note:

1. Signal usage in PIO & Multiword DMA mode.
2. Signal usage in Ultra DMA mode

2. Theory of operation

2.1 Overview

Figure 2 shows FiD ATA4000 operation from the system level, including the major hardware blocks.

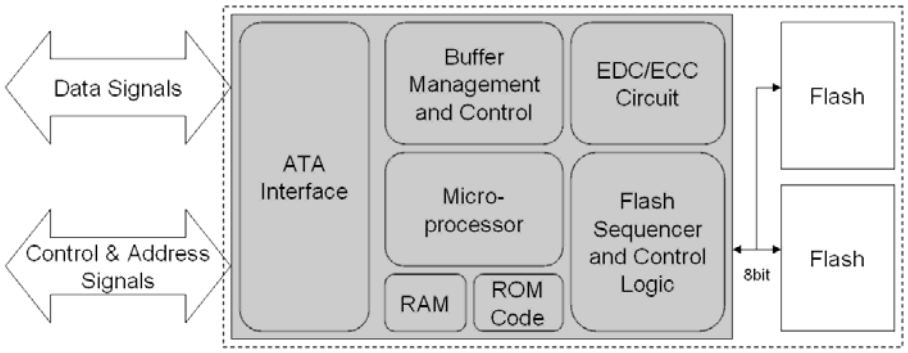


Figure 2: FiD ATA4000 Block Diagram

FiD ATA4000 integrates an IDE controller and flash devices. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

2.2 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit

(parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements a Reed-Solomon algorithm that can correct two bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.3 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

FiD ATA4000 uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

3. Specifications

3.1 CE and FCC Compatibility

FiD ATA4000 conforms to CE requirements and FCC standards.

3.2 RoHS Supports

FiD ATA4000 is fully compliant with RoHS directive.

3.3 Environmental Specification

3.3.1 Temperature Ranges

Temperature Range: -10°C to +70°C

Storage Temperature: -40°C to +85°C

3.3.2 Humidity

Relative Humidity: 10-95%, non-condensing

3.3.3 Shock and Vibration

Table 3: Shock/Vibration Testing for FiD ATA4000

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 700Hz, 2 g, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms,1 500 g, 3 axes	IEC 68-2-27
Drop Unit	From a height of 1.5 m	IEC 68-2-32

3.3.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various FiD ATA4000 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

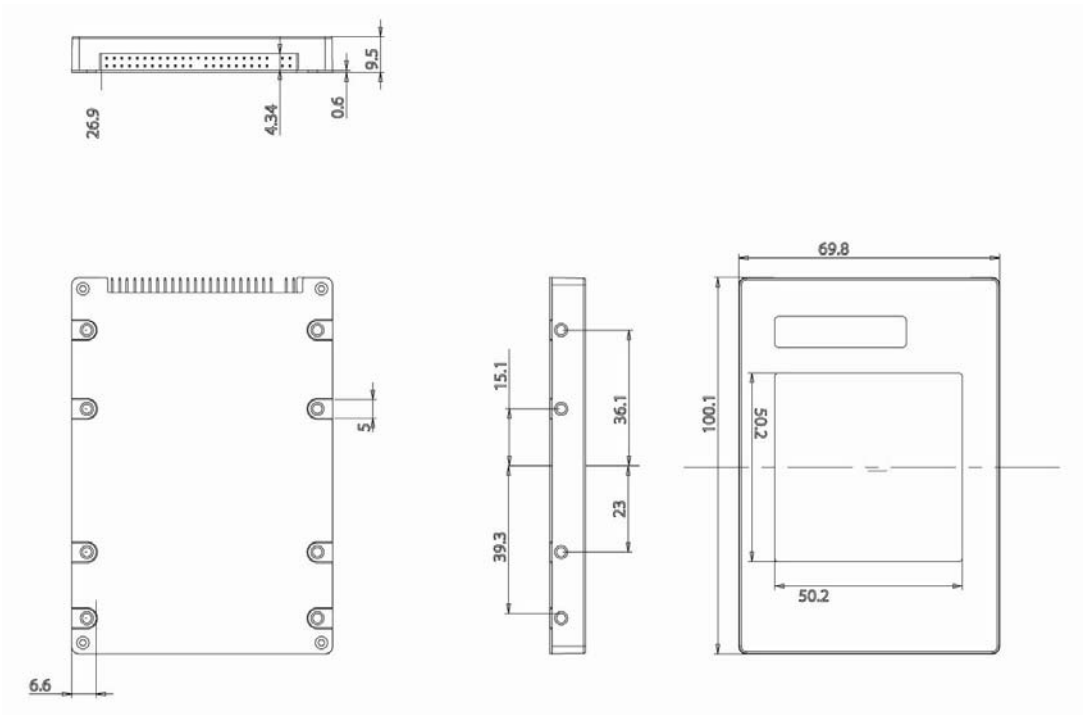
Table 4: FiD ATA4000 MTBF

Product	Condition	MTBF (Hours)
FiD ATA4000	Telcordia SR-332 GB, 25 °C	> 3,000,000

3.4 Mechanical Dimensions

Mechanical Dimension: 100.1/69.8/9.5 mm (W/T/H)

Figure 3: Mechanical Dimension of FiD ATA4000



3.5 Timing Specifications

3.5.1 PIO Mode

Figure 4: Read/Write Timing Diagram, PIO Mode

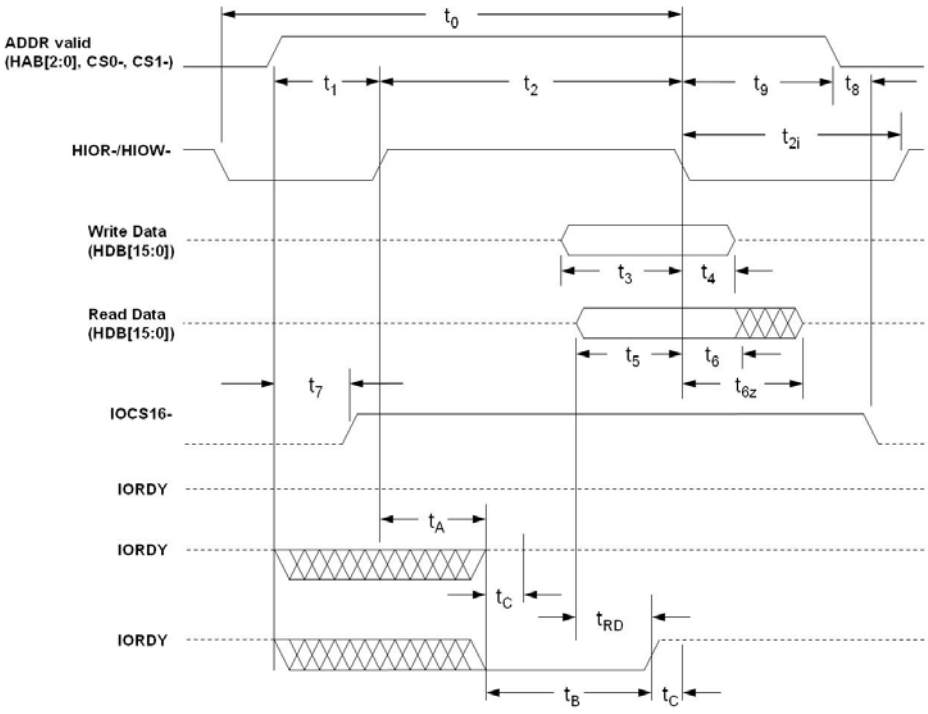


Table 5: Read/Write Timing Specifications, PIO Mode 0-4

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_0	Cycle time (min.)	600	383	240	180	120
t_1	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25
t_2	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70
t_{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25
t_3	HIOW- data setup (min.)	60	45	30	30	20
t_4	HIOW- data hold (min.)	30	20	15	10	10
t_5	HIOR- data setup (min.)	50	35	20	20	20
t_6	HIOR- data hold (min.)	5	5	5	5	5
t_{6z}	HIOR- data tri-state (max.)	30	30	30	30	30
t_7	Address valid to IOCS16- assertion (max.)	90	50	40	n/a	n/a
t_8	Address valid to IOCS16- released (max.)	60	45	30	n/a	n/a
t_9	HIOR-/HIOW- to address valid hold	20	15	10	10	10
t_{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0
t_A	IORDY setup time	35	35	35	35	35
t_B	IORDY pulse width (max.)	1250	1250	1250	1250	1250
t_C	IORDY assertion to release (max.)	5	5	5	5	5

3.5.2 Multiword Mode

Figure 5: Read/Write Timing Diagram, Multiword DMA Mode

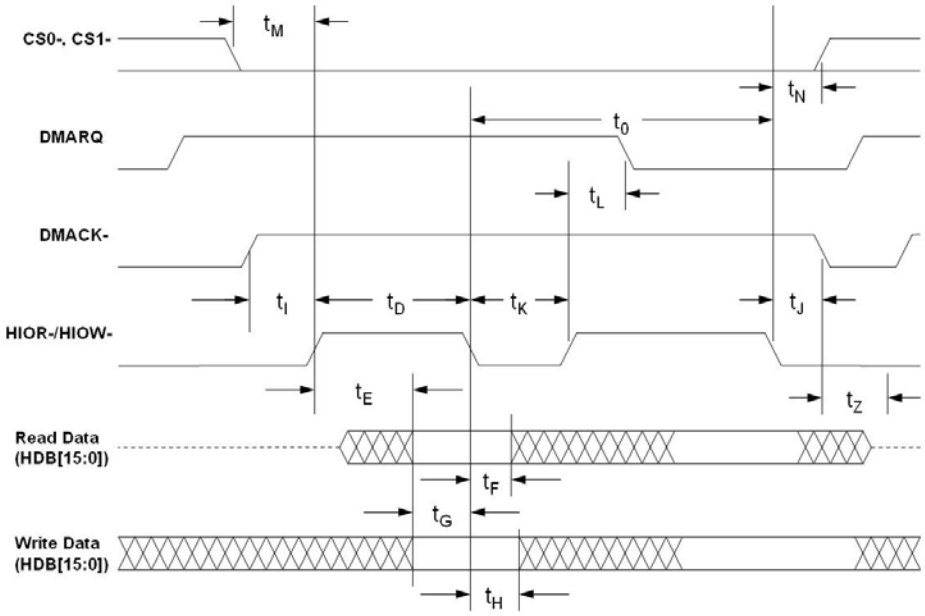


Table 6: Read/Write Timing Specifications, Multiword DMA Mode 0-2

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2
t_0	Cycle time (min.)	480	150	120
t_D	HIOR-/HIOW- assertion width (min.)	215	80	70
t_E	HIOR- data access (max.)	150	60	50
t_F	HIOR- data hold (min.)	5	5	5

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2
t_G	HIOR-/HIOW- data setup (min.)	100	30	20
t_H	HIOW- data hold (min.)	20	15	10
t_I	DMACK to HIOR-/HIOW- setup (min.)	0	0	0
t_J	HIOR-/HIOW- to DMACK hold (min.)	20	5	5
t_{KR}	HIOR- negated width (min.)	50	50	25
t_{KW}	HIOW- negated width (min.)	215	50	25
t_{LR}	HIOR- to DMARQ delay (max.)	120	40	35
t_{LW}	HIOW- to DMARQ delay (max.)	40	40	35
t_M	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25
t_N	CS1-, CS0- hold	15	10	10
t_Z	DMACK-	20	25	25

3.5.3 Ultra DMA Mode

Figure 6: Ultra DMA Mode Data-in Burst Initiation Timing Diagram

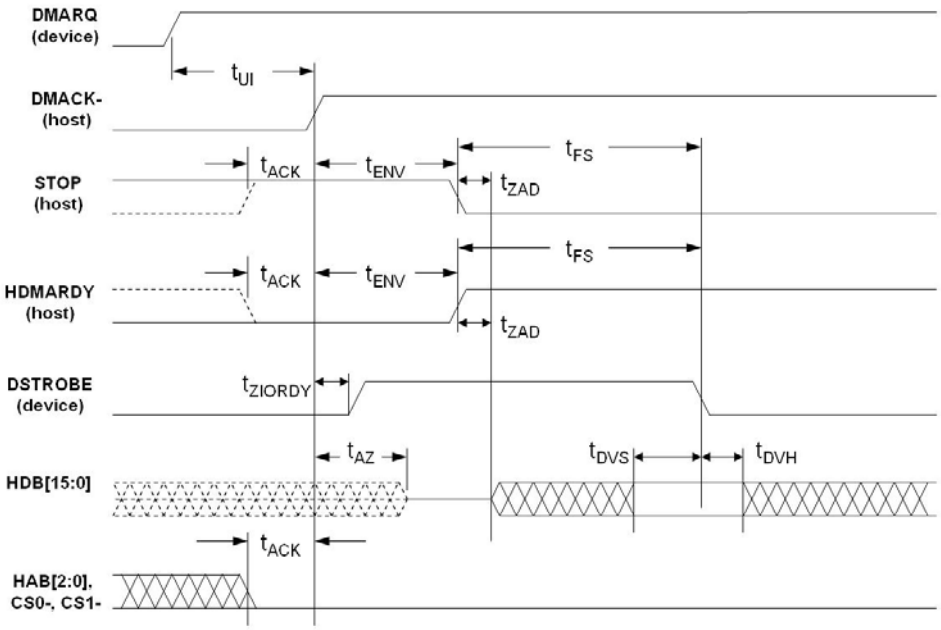


Figure 7: Ultra DMA Mode Data-out Burst Initiation Timing Diagram

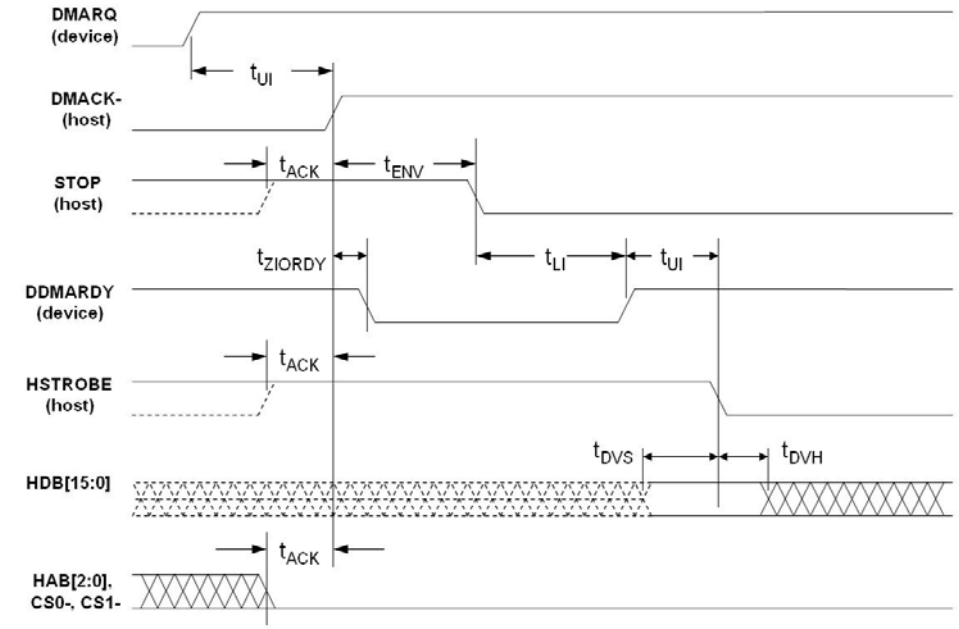


Figure 8: Sustained Ultra DMA Mode Data-in Burst Timing Diagram

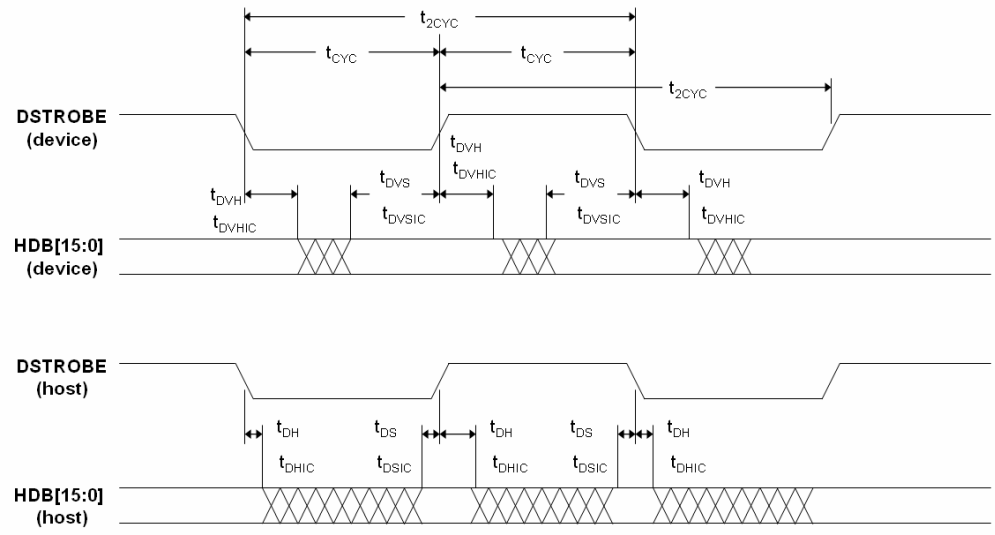


Figure 9: Sustained Ultra DMA Mode Data-out Burst Timing Diagram

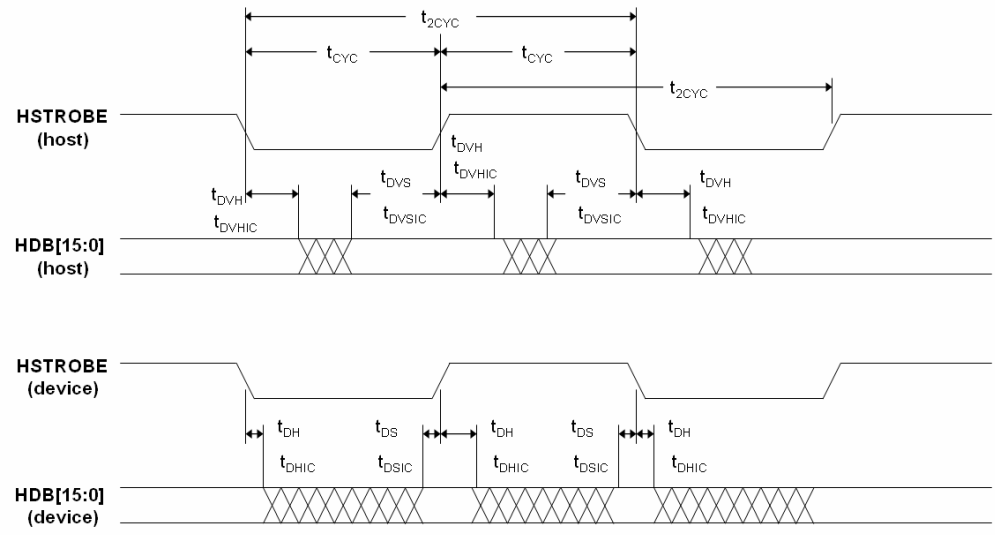


Table 7: Timing Diagram, Ultra DMA Mode 0-2

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2	
		Min.	Max.	Min.	Max.	Min.	Max.
t_{2CYC}	Typical sustained average two cycle time	240	-	160	-	120	-
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	114	-	75	-	55	-
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	235	-	156	-	117	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	34	-
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6	-	6	-	6	-
t_{FS}	First STROBE time (for device to first negate	0	230	0	200	0	170
t_{LI}	Limited interlock time	0	150	0	150	0	150
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-
t_{UI}	Unlimited interlock time	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10
t_{ZAH}	Minimum delay time required for output	20	-	20	-	20	-
t_{ZAD}	drivers to assert or negate (from released state)	0	-	0	-	0	-
t_{ENV}	Envelope time (from DMACK- to STOP and	20	70	20	70	20	70
t_{SR}	STROBE to DMARDY time (if DMARDY- is negated before this long after STROBE edge, the recipient shall	-	50	-	30	-	20
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	60	-	50
t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender	50		50	-	50	-

3.6 Supported IDE Commands

FiD ATA4000 supports the commands listed in Table 8.

Table 8: IDE Commands

Command Name	Command Code
Check Power Mode	98H or E5H
Execute Device Diagnostic	90H

Command Name	Command Code
Erase Sector	C0H
Flush Cache	E7H
Format Track	50H
Identify Device	ECH
Idle	97H or E3H
Idle immediate	95H or E1H
Initialize Device Parameters	91H
NOP	00H
Read Buffer	E4H
Read Long Sector	22H or 23H
Read Multiple	C4H
Read Sector	20H or 21H
Read Verify Sector	40H or 41H
Recalibrate	1XH
Seek	7XH
Set Features	EFH
Set Multiple Mode	C6H
Set Sleep Mode	99H or E6H
Standby	96H or E2H
Standby Immediate	94H or E0H
Write Buffer	E8H
Write Long Sector	E8H
Write Multiple	C5H
Write Sector	30H or 31H
Write Verify	3CH