InnoDisk FiD2.5” ATA6000

Flash in Disk 2.5” ATA6000

Datasheet

Preliminary

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REVISION HISTORY

Revision	Description	Date
0.0	Release Preliminary	January 2008

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1. Product Overview

1.1 Introduction to Flash in Disk

Flash in Disk (FiD) 2.5” ATA6000 products provide high capacity 2.5-inch solid-state flash disk that electrically complies with ATA6 standard. InnoDisk FiD 2.5” ATA6000 is 2.5-inch solid-state data storage systems under industrial environment.

FiD 2.5” ATA6000 supports PIO(0-4), Multiword DMA(0-2) and Ultra DMA(0-5) transfer modes. FiD 2.5” ATA6000 supports LBA addressing mode.

1.2 Pin Assignments

FiD 2.5” ATA6000 uses a standard IDE 44-pin. See Figure 1 & Table 1 for FiD 2.5” ATA6000 pin assignments.

Figure 1: FiD 2.5” ATA6000 Connector Layout

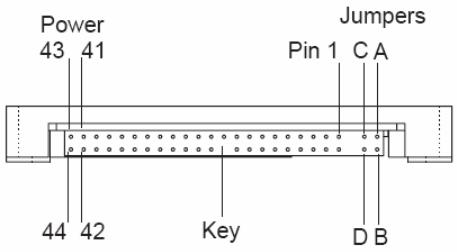


Table 1: FiD 2.5” ATA6000 Pin Assignment

Pin No.	Name	Function	Pin No.	Name	Function
1	HRESET	Host Reset	2	GND	Ground
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11

11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15
19	GND	Ground	20	KEY	Key-pin
21	DMARQ	DMA Request	22	GND	Ground
	HIOW[1]	Host I/O Write			
23	STOP[2]	Stop Ultra DMA burst	24	GND	Ground
	HIOR[1]	Host I/O Read			
	HDMARDY[2]	Ultra DMA ready			
25	HSTROBE[2]	Ultra DMA data strobe	26	GND	Ground

Pin No.	Name	Function	Pin No.	Name	Function
	IORDY[1]	I/O Ready			
	DDMARDY[2]	Ultra DMA ready			
27	DSTROBE[2]	Ultra DMA data strobe	28	CSEL	Master/Slave Select
29	DMACK	DMA Acknowledge	30	GND	Ground
31	INTRQ	Interrupt Request	32	IOCS16	CS I/O 16-Bit
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic
35	HAB[0]	Host Address Bit 0	36	HAB[2]	Host Address Bit 2
37	CS0	Chip Select 0	38	CS1	Chip Select 1
39	DASP	Drive Active	40	GND	Ground
41	VCC	Supply Voltage	42	VCC	Supply Voltage
43	GND	Ground	44	NC	Not Connected
A	N/A	Master/Slave	B	N/A	Master/Slave
C	N/A	NC	D	N/A	NC

Note: 1. Signal usage in PIO & Multiword DMA mode.

2. Signal usage in Ultra DMA mode.

1.3 Pin Descriptions

Table 2 describes the pin descriptions for FiD 2.5” ATA6000

Table 2: FiD 2.5” ATA6000 Pin Descriptions

Host side			
HRESET-	1	Host reset signal, High: Reset.	I
CS0-	37	Chip select CS0	I
CS1-	38	Chip select CS1	I
INTRQ	31	Host interrupt signal.	O
HIOR-[1]		I/O read strobe signal.	
HDMARDY-[2]		DMA ready during Ultra DMA data in burst	

HSTROBE[2]		Data strobe during Ultra DMA data out burst	
HIOW-[1]	23	I/O write strobe signal.	I
STOP[2]		Stop during Ultra DMA data bursts	
IOCS16-	32	Asserted in 16-bit access.	O
IORDY[1]	27	I/O Ready Signal	O
DDMARDY-[2]		DMA ready during Ultra DMA data out burst	
DSTROBE[2]		Data strobe during Ultra DMA data in burst	
HDB[15:0]	18, 16, 14, 12, 10, 8, 6, 4, 3, 5,	Host data bus	I/
HAB[2:0]	33, 35,	Host Address bus	I/
CSEL-	28	Master/Slave select signal (cable select signal).	I
DASP-	39	Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.	I/
Pin Name	**Pin**	**Descriptio**	**I/**
PDIAG-	34	Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.	I/
DMARQ	21	DMA Request.	O
DMACK-	2	DMA Acknowledge.	I
Power and			
VCC	41,	Connect to VCC	VCC
GND	2, 19, 22, 24, 26, 30, 40,	Connect to GND.	GND
Other			
KEY	20	Key-Pin	N/A
Master/Slave	A,	Master/Slave	N/A
NC	44, C,	Not used. Please do not connect.	N/A

Note:

1. Signal usage in PIO & Multiword DMA mode.
2. Signal usage in Ultra DMA mode

2. Theory of operation

2.1 Overview

Figure 2 shows FiD 2.5” ATA6000 operation from the system level, including the major hardware blocks.

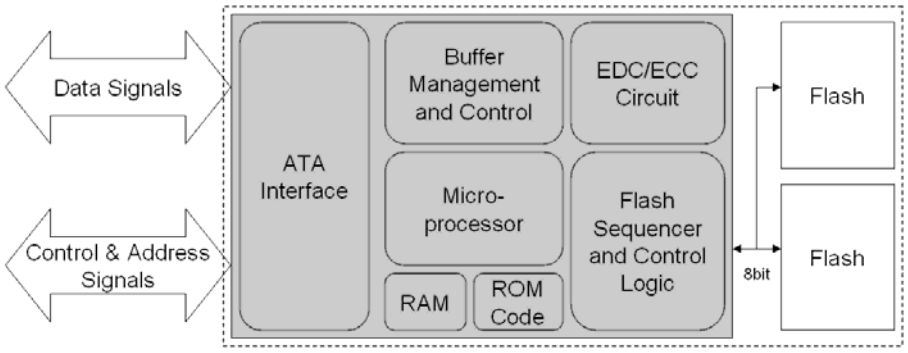


Figure 2: FiD 2.5” ATA6000 Block Diagram

FiD 2.5” ATA6000 integrates an IDE controller and flash devices. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

2.2 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements a BCH algorithm that can correct four bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.3 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

FiD 2.5” ATA6000 uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page in the flash. This averages flash media usage evenly across all pages, thereby flash lifetime extends.

3. Specifications

3.1 CE and FCC Compatibility

FiD 2.5” ATA6000 is approved for CE requirements and FCC standards.

3.2 RoHS Supports

FiD 2.5” ATA6000 is fully compliant with RoHS directive, also known as Restriction of Hazardous Substances directive.

3.3 Performance

Burst Transfer Rate : 100MB/sec (UDMA5)
Sustained Read : 60MB/sec
Sustained Write : 40MB/sec
Average Latency : 0.4 ms
Notes- InnoDisk FiD 2.5”SATA 6000 is not a magnetic rotating design. There is no seek or rotational latency required.

3.4 Environmental Specification

3.4.1 Temperature Ranges

Operation Temperature Range: -10°C to +70°C
Storage Temperature : -55°C to +95°C

3.4.2 Humidity

Relative Humidity: 10-95%, non-condensing

3.4.3 Shock and Vibration

Table 3: Shock/Vibration for FiD 2.5” ATA6000

Vibration	7 Hz to 700Hz, 2 g, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms,1 500 g, 3 axes	IEC 68-2-27
Drop Unit	From a height of 1.5 m	IEC 68-2-32

3.4.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various FiD 2.5” ATA6000 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

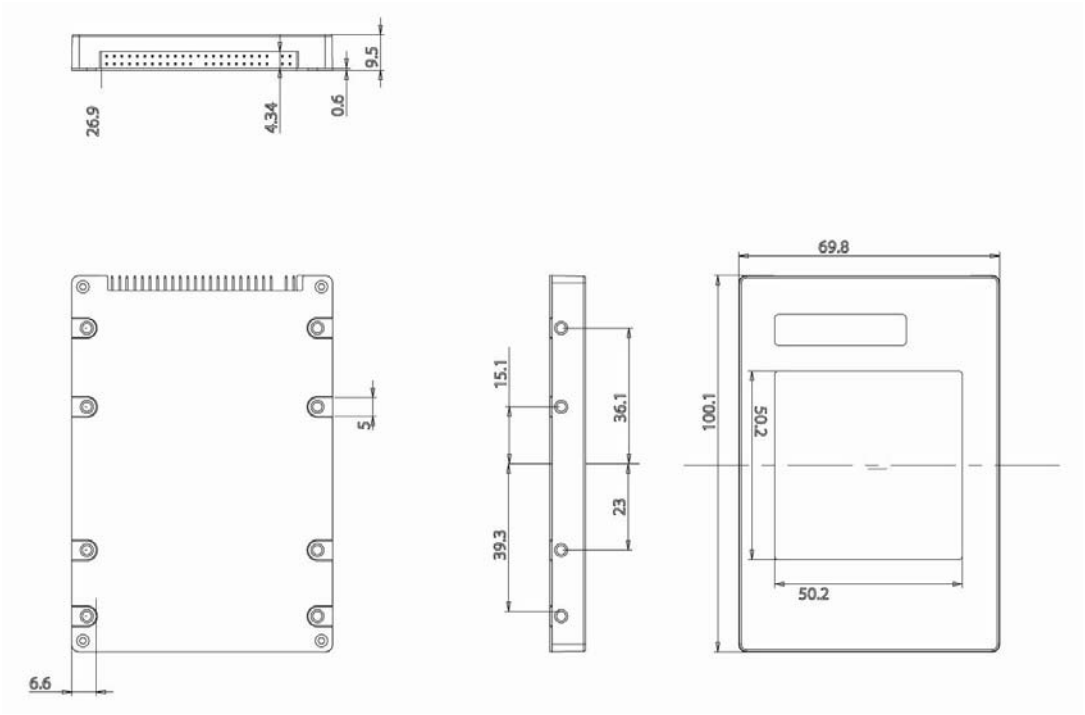
Table 4: FiD 2.5” ATA6000 MTBF

FiD 2.5” ATA6000	Telcordia SR-332 GB, 25 °C	> 3,000,000

3.5 Mechanical Dimensions

Mechanical Dimension: 100.1/69.8/9.5 mm (W/T/H)

Figure 3: Mechanical Dimension of FiD 2.5” ATA6000



4 Timing Specifications

4.1 Deskewing

For PIO and Multiword DMA modes all timing values shall be measured at the connector of the selected device. The host account cable skew.

For Ultra DMA modes unless otherwise specified, timing parameters shall be measured at the connector of the host or device which the parameter applies.

4.2 Transfer timing

The minimum cycle time supported by the device (FiD 2.5” ATA6000) in PIO mode 3,4 and Multiword DMA mode 1,2 respectively always be greater than or equal to the minimum cycle time defined by the associated mode e.g., a device supporting PIO mode 4 timing shall not report a value less than 120 ns, the minimum cycle time defined for PIO mode 4 timings.

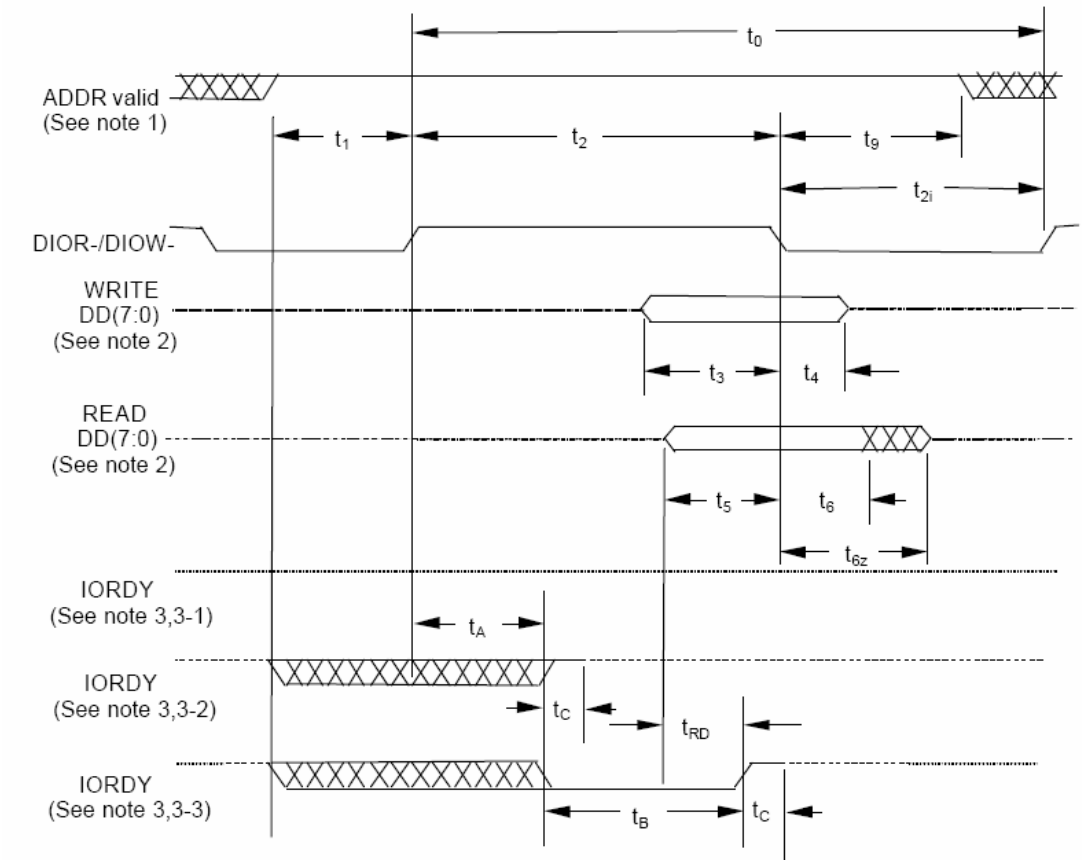
4.2.1 Register transfers

Figure 4 defines the relationships between the interface signals for register transfers. Peripherals reporting support for PIO mode 3 or 4 shall power-up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 5 defines the minimum value that shall be placed in word 68.

Hosts shall support IORDY when PIO mode 3 or 4 are the currently selected mode of operation.

Figure 4 – Register Transfer to/from device



Notes –

Device address consists of signals CS0-, CS1-, and DA(2:0)

Data consists of DD(7:0)

The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of DIOR- or DIOW-, The assertion and negation of IORDY are described in the following three cases:

3-1 Device never negates IORDY, device keeps IORDY released: no wait is generated.

3-2 Device negates IORDY before tA , but cases IORDY to be asserted before tA . IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.

3-3 Device negates IORDY before tA . IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR-

is asserted, the device shall place read data on DD(7:0) for tRD before asserting IORDY.

4. DMACK- shall remain negated during a register transfer.

Table 5- Register transfer to/from device

Register transfer timing parameters		Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle Time (min)	600	383	330	180	120	1,4,5
t_1	Address valid to DIOR-/DIOW-setup (min)	70	50	30	30	25	
t_2	DIOR-/DIOW – pulse width 8-bit (min)	290	290	290	80	70	1
t_{2i}	DIOR-/DIOW – recovery time (min)	-	-	-	70	25	1
t_3	DIOW- data setup (min)	60	45	30	30	20	
t_4	DIOW- data hold (min)	30	20	15	10	10	
t_5	DIOR- data setup (min)	50	35	20	20	20	
t_6	DIOR – data hold (min)	5	5	5	5	5	
T_{6z}	DIOR – data tristate (max)	30	30	30	30	30	2
T_9	DIOR-/DIOW- to address valid (min)	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (min) (if IORDY initially low after t_A)	0	0	0	0	0	
t_A	IORDY Setup time	35	35	35	35	35	3
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release (max)	5	5	5	5	5	

.Notes-

1 t0 is the minimum total cycle time, t2 is the minimum DIOR-/DIOW – assertion time, and t2i is the minimum DIOR-/DIOW – negation time. A host implementation shall lengthen t2 and/or t2i to ensure that t0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2. This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is released by the device.

3. The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the register transfer cycle is completed. If the device is not driving IORDY negated at the

tA after the activation of DIOR- or DIOW-, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then tRD shall be met and t5 is not applicable.

4. ATA/ATAPI standards prior to ATA/ATAPI-5 inadvertently specified an incorrect value for mode 2 time t0 by utilizing the 16-bit PIO value.

5. Mode shall be selected no faster than the highest mode supported by the slowest device.

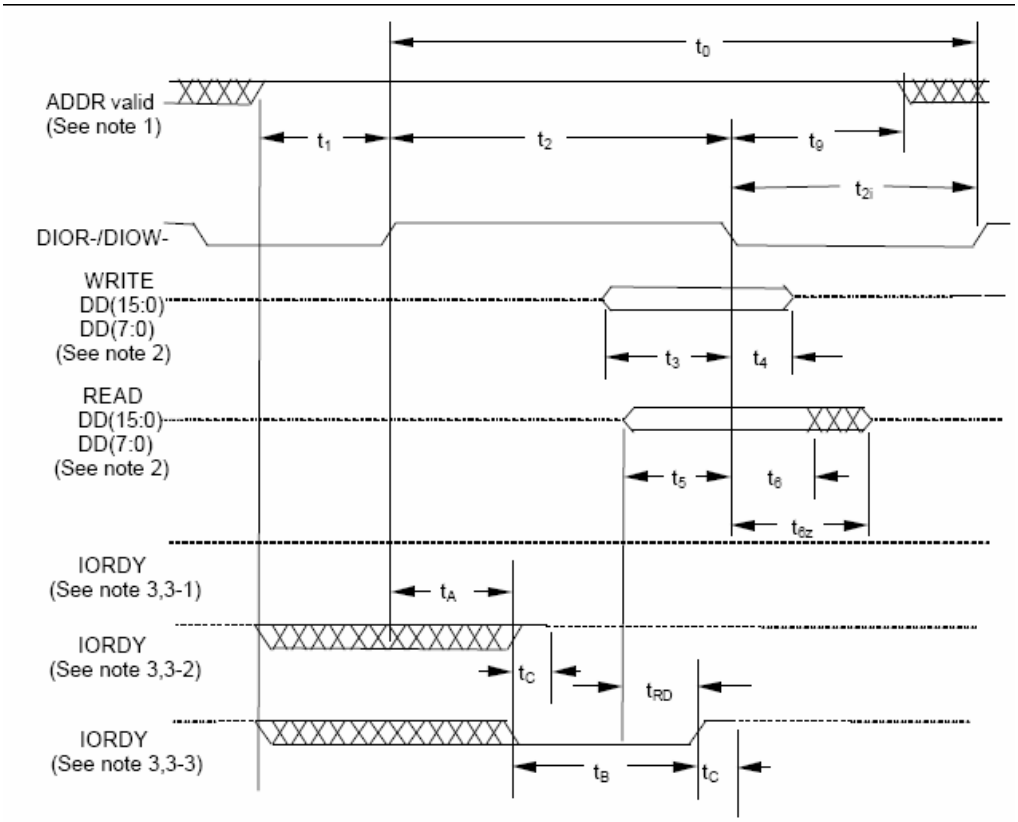
4.4.2 PIO data transfers

Figure 5 defines the relationships between the interface signals for PIO data transfer. Peripherals reporting support for PIO mode 3 or 4 shall power-up in a PIO mode 0, 1 or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 6 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO mode 3 or 4 are the current mode of operation.

Figure 5 – PIO data transfer to/from device



NOTES –

Device address consists of signals CS0-, CS1-, and DA(2:0)

Data consists of DD(15:0) for all devices.

The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended us made by the host after tA from the assertion of DIOR- or DIOW-.

The assertion and negation of IORDY are described in the following three cases:

3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.

3-2 Device negates IORDY before tA, but causes IORDY to be asserted before tA. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.

3-3 Device negates IORDY before tA. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes

after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place data on DD(7:0) for tRD before asserting IORDY.

DMACK- shall be negated during a PIO data transfer.

Table 6 – PIO data transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Modes 4 ns	Note
t_0	Cycle Time	(min)	600	383	240	180	120	1,4
t_1	Address valid to DIOR-/DIOW-setup	(min)	70	50	30	30	25	
t_2	DIOR-/DIOW –	(min)	165	125	100	80	70	1
t_{2i}	DIOR-/DIOW – recovery time	(min)	-	-	-	70	25	1
t_3	DIOW- data setup	(min)	60	45	30	30	20	
t_4	DIOW- data hold	(min)	30	20	15	10	10	
t_5	DIOR- data setup	(min)	50	35	20	20	20	
t_6	DIOR – data hold	(min)	5	5	5	5	5	
T_{6Z}	DIOR – data release	(max)	30	30	30	30	30	2
T_9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	(min)	0	0	0	0	0	
t_A	IORDY Setup time		35	35	35	35	35	3
t_B	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release	(max)	5	5	5	5	5	

Notes-

1 t0 is the minimum total cycle time, t2 is the minimum DIOR-/DIOW – assertion time, and t2i is the minimum DIOR-/DIOW – negation time. A host implementation shall lengthen t2 and/or t2i to ensure that t0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. FiD2.5” ATA6000 supports any legal host implementation.

2. This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is released by the device.

3. The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the register transfer cycle is completed. If the device is not driving IORDY negated at the

tA after the activation of DIOR- or DIOW-, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then tRD shall be met and t5 is not applicable.

4. Mode may be selected at the highest mode for the device if CS(1:0) and DA(2:0) do not change between read or write cycles or selected at the highest mode supported by the slowest device if CS(1:0) or DA(2:0) do change between read or write cycles.

4.4.3 Multiword DMA data transfer

Figure 6 through Figure 9 define the timing associated with Multiword DMA transfers. For multiword DMA modes 1 and above, the minimum value of t_0 is specified by word 65 in the IDEENTIFY DEVICE parameter list. Table 7 defines the minimum value that shall be placed in word 65.

Devices shall power-up with mode 0 as the default Multiword DMA mode.

Table 7 – Multiword DMA data transfer

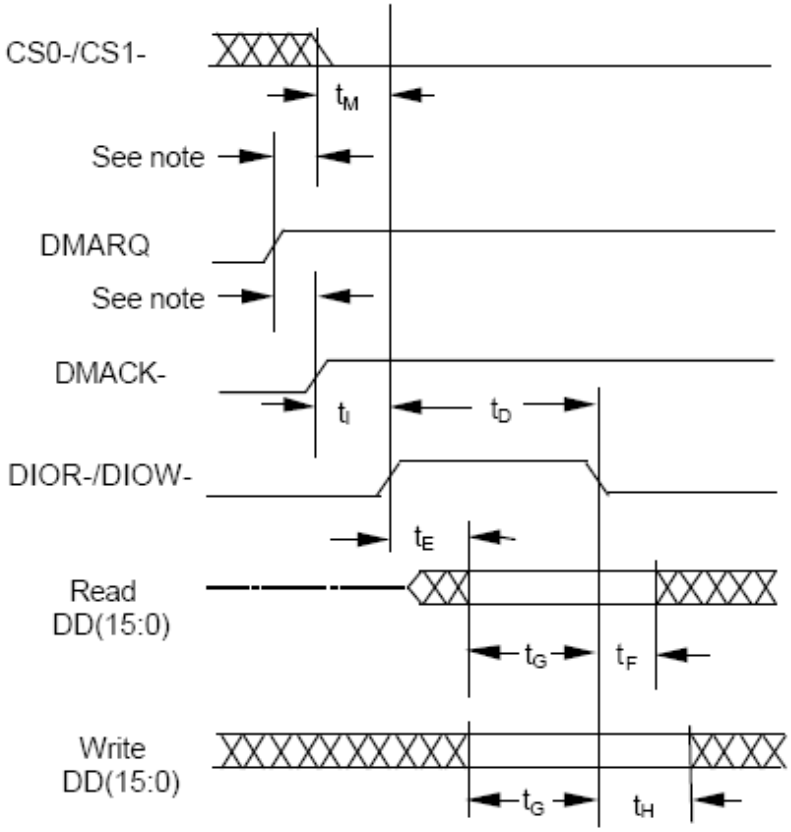
Multiword DMA timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Note
t_0	Cycle Time	(min)	480	150	120	See note
t_D	DIOR-/DIOW- asserted pulse width	(min)	215	80	70	See note
t_E	DIOR- data access	(min)	150	60	50	
t_F	DIOR- data hold	(min)	5	5	5	
t_G	DIOR- /DIOW data setup	(min)	100	30	20	
t_H	DIOW- data hold	(min)	20	15	10	
t_I	DMACK to DIOR-/DIOW – setup	(min)	0	0	0	
t_J	DIOR-/DIOW – to DMACK hold	(min)	20	5	5	
t_{KR}	DIOW – negated pulse width	(max)	50	50	25	See note
t_{KW}	DIOW- negated pulse width	(min)	215	50	25	See note
t_{LR}	DIOR- to DMARQ delay	(min)	120	40	35	
t_{LW}	DIOW- to DMARQ delay	(min)	40	40	35	
t_M	CS(1:0) valid to DIOR-/DIOW-	(max)	50	3	25	
t_N	CS(1:0) hold	(max)	15	10	10	
t_Z	DMACK- to read data released	(max)	20	25	25	

Notes- t_0 is the minimum total cycle time, t_D is the minimum DIOR-/DIOW- assertion time, and t_K (t_{KR} or t_{KW}, as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen t_D and/or t_K to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data.

4.4.3.1 Initiating a Multiword DMA data burst

The Values for the timings for each of the Multiword DMA modes are contained in Table 7.

Figure6 – Initiating a Multiword DMA data burst

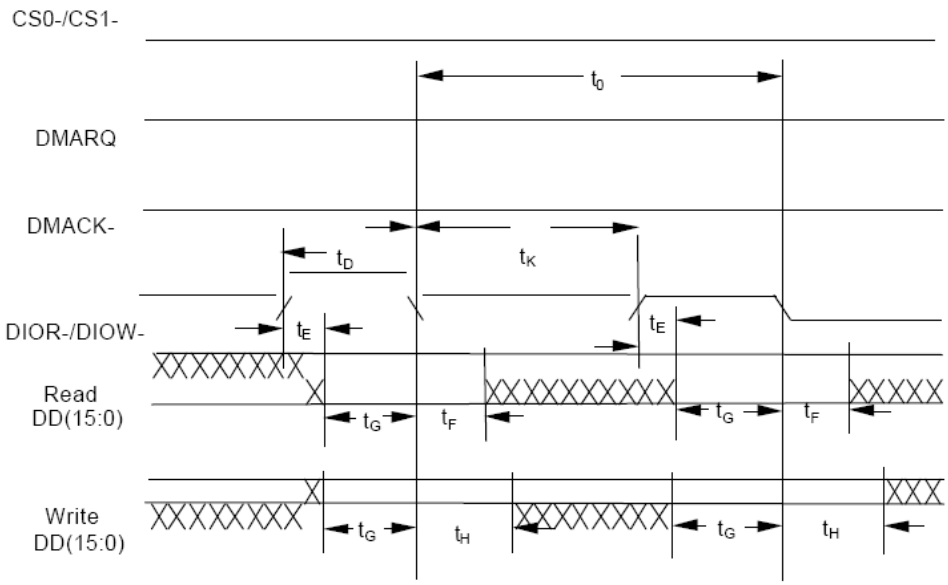


Note –The host shall not assert DMACK- or negate both CS0 and CS1 until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK- or the negation of both CS0 and CS1 is not defined.

4.4.3.2 Sustaining a Multiword DMA data burst

The values for the timings for each of the Multiword DMA modes are contained in Table 7.

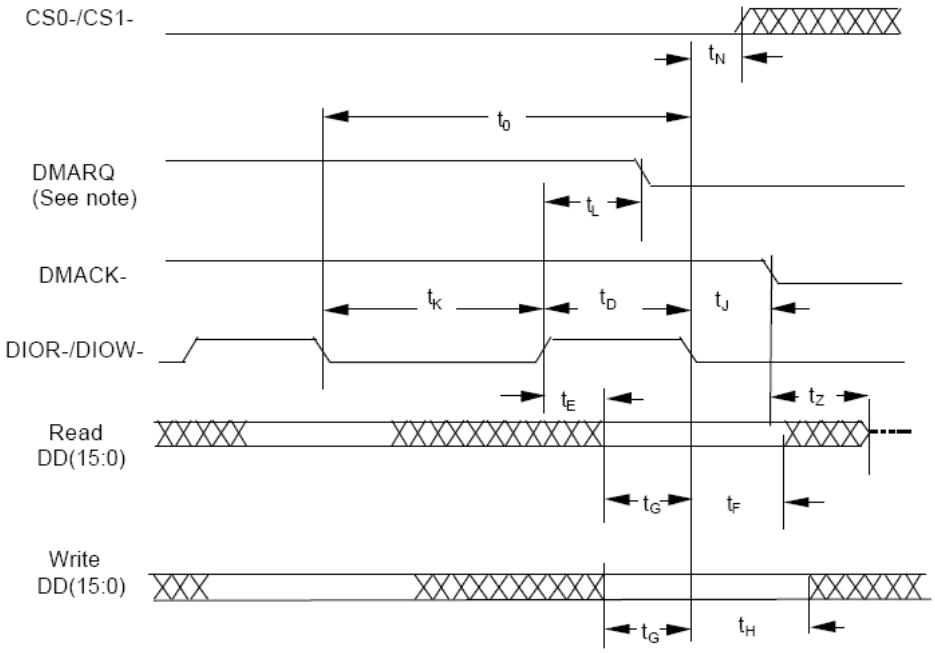
Figure 7- Sustaining a Multiword DMA data burst.



4.4.3.3 Device terminating a Multiword DMA data burst

The values for the timings for each of the Multiword DMA modes are contained in Table 7.

Figure 8- Device terminating a Multiword DMA data burst

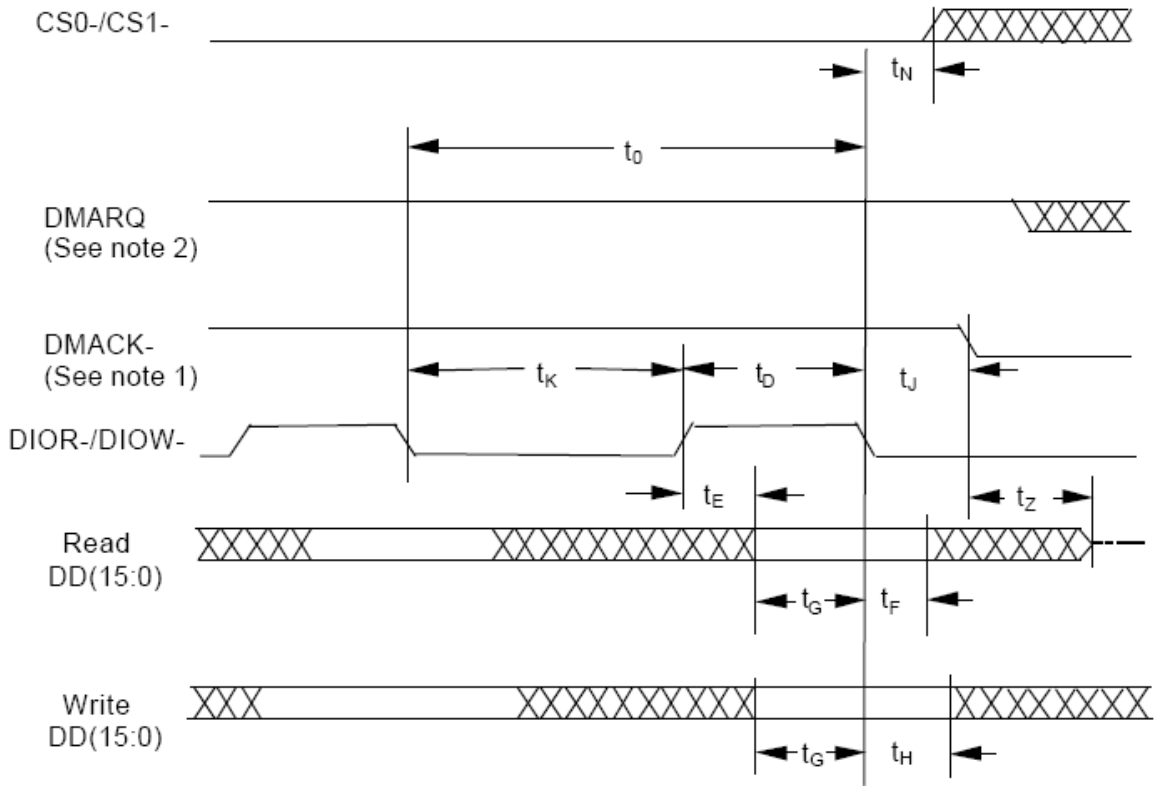


Note- To terminate the data burst, the device will negate DMARQ within tL of the assertion of the current DIOR- or DIOW- pulse. The last data word for the burst will then be transferred by the negation of the current DIOR- or DIOW- pulse. If all data for the command has not been transferred, the device will assert DMARQ again at any later time to resume the DMA operation as shown in figure 5.

4.4.3.4 Host terminating a Multiword DMA data burst

The values for the timings for each of the Multiword DMA modes are contained in Table 7

Figure 9- Host terminating a Multiword DMA data burst



Note-

1. To terminate the transmission of a data burst, the host will negate DMACK- within tJ after a DIOR- or DIOW- pulse. No further DIOR- or DIOW- pulses will be asserted for this burst,

2. If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK- or may negate DMARQ at any time after detecting that DMACK- has been negated.

4.4.4 Ultra DMA data transfer

Figure 10 through Figure 19 define the timings associated with all phases of Ultra DMA bursts. Table 8 contains the values for the timings fir each of the Ultra DMA modes. Table 9 contains descriptions and comments for each of the timing values in Table 8. Table 10 contains timings specified for the IC alone.

All timing measurement switching points (low to high and high to low) shall be taken at 1.5V.

Table 8 – Ultra DMA data burst timing requirements

Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Mode 5 (in ns)		Measurement Location.
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t2cyctype	240		160		120		90		60		40		Sender
tcyc	112		73		54		39		25		16.8		Recipient
t2cyc	230		153		115		86		57		38		Sender
tds	15.0		10.0		7.0		7.0		5.0		4.0		Recipient
tdh	5.0		5.0		5.0		5.0		5.0		4.6		Recipient
tdvs	70.0		48.0		31.0		20.0		6.7		4.8		Sender
tdvh	6.2		6.2		6.2		6.2		6.2		4.8		Sender
tcs	15.0		10.5		7.0		7.0		5.0		5.0		Device
tch	5.0		5.0		5.0		5.0		5.0		5.0		Device
tcvs	70.0		48.0		31.0		20.0		6.7		10.0		Host
tcvh	6.2		6.2		6.2		6.2		6.2		10.0		Host
tzfs	0		0		0		0		0		35		Device
tdzfs	70.0		48.0		31.0		20.0		6.7		25		Sender
tfs		230		200				130		120		90	Device
tli	0	150	0	150	0		0	100	0	100	0	75	Note2
tmli	20		20		20		20		20		20		Host
tui	0		0		0		0		0		0		Host
taz		10		10		10		10		10		10	Note3
tzah	20		20		20		20		20		20		Host
tzad	0		0										Device
tenv	20	70	20	70	20	70	20	55	20	55	20	50	Host
trfs		75		70		60		60		60		50	Sender
trp	160		125		100		100		100		85		Recipient
tiordyz		20		20		20		20		20		20	Device

tziordy	0		0		0		0		0		0		Device
tack	20		20		20		20		20		20		Host
tss	50		50		50		50		50		50		Sender

Notes –

All Signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and DMARDY- transitions are measured at the sender connector.

The parameter tLI shall be measured at the connector of the sender of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

The parameter tAZ shall be measured at the connector of the sender or recipient that is releasing the bus.

Table 9 – Ultra DMA data burst timing descriptions

Name	Comment
t_{2CYCTY}	Typical sustained average two cycles time
t_{CYC}	Cycle time allowing asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	Data setup time at recipient (from data valid until STROBE edge) (see note2,5)
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid) (see note 2,5)
t_{DVS}	Data valid setup time at sender(from data valid until STROBE edge) (see note3)
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid) (see note3)
t_{CS}	CRC word setup time at device (see note2)
t_{CH}	CRC word hold time device(see note2)
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK – negation) (see note3)
t_{CVH}	CRC word valid hold time at sender (from DMACK-negation until CRC may become invalid) (see note3)
t_{ZFS}	Time from STROBE output released-to driving until the first transition of critical timing.
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timeing.
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	Limited interlock time (see note1)
t_{MLI}	Interlock time with minimum (see note1)
t_{UI}	Unlimited interlock time (see note1)
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	Minimum delay time required for output
t_{ZAD}	Drivers to assert or negate(from released)
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY – during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{RFS}	Ready –to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)
t_{IORDYZ}	Maximum time before releasing IORDY
t_{ZIORDY}	Minimum time before driving IORDY (see note4)
t_{ACK}	Setup and hold times for DMACK-(before assertion or negation)
t_{SS}	Time from STROBE edge to negation of DMACK of DMARQ or assertion of STOP (when sender terminates a burst)
NOTES-	

The parameters tUI, tMLI (in figure 13 and Figure 14), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum.

80-conductor cabling shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2.

Timing for tDVS, tDVH, tCVS and tVCH shall be met for lumped capacitive loads of 15 and 40 of at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable. These timing measurements are not valid in a normally functioning system.

For all modes the parameter tZIORDY may be greater than tENV due to the fact that the host a pull-up on IORDY- giving it a known state when released.

The parameter tDS, and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with one device at the end of the cable.

Table 10- Ultra DMA sender and recipient IC timing requirements

Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Mode 5 (in ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	**14.7**		**9.7**		**6.8**		**6.8**		**4.8**		**2.3**	
t_{DHIC}	**4.8**		**4.8**		**4.8**		**4.8**		**4.8**		**2.8**	
t_{DVSIC}	**72.9**		**50.9**		**33.9**		**22.6**		**9.5**		**6.0**	
t_{DVHIC}	**9.0**		**9.0**		**9.0**		**9.0**		**9.0**		**6.0**	

	Comment
t_{DSIC}	**Recipient IC data setup time (from data valid until STROBE edge) (see note1)**
t_{DHIC}	**Recipient IC data hold time (from STROBE edge until data may become invalid) (see note1)**
t_{DVSIC}	**Sender IC data valid setup time (from data valid until STROBE edge) (see note2)**
t_{DVHIC}	**Sender IC data valid hold time(from STROBE edge until data may become invalid) (see note3)**

NOTES-

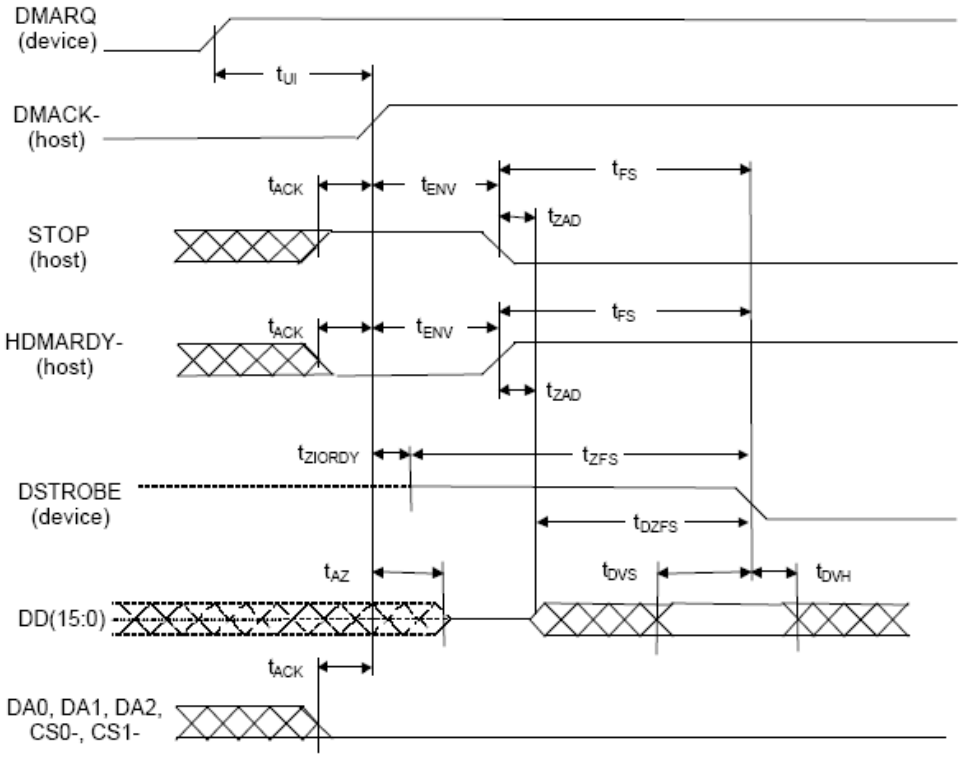
The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDISC and tDHIC timing (as measured throuth 1.5V)

The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pf at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources in a normally functioning system has not been included in these values.

4.4.4.1 Initiating an Ultra DAM data-in burst

The value for the timings for each of the Ultra DMA modes are contained in 4.4.4

Figure 10- Initiating an Ultra DMA data-in burst



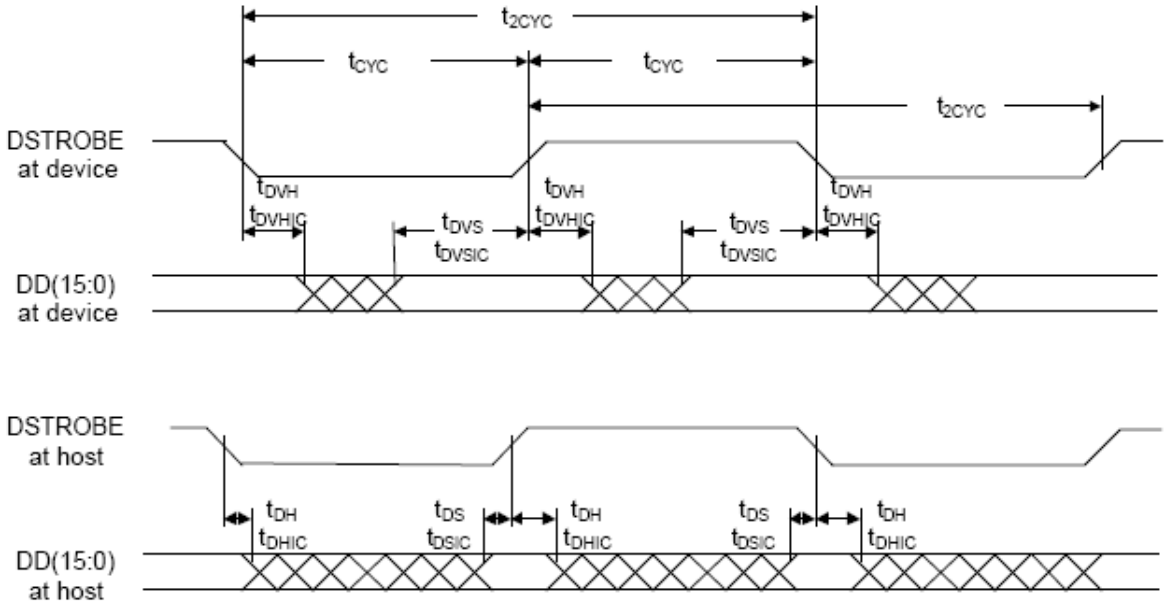
Notes-

1. The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE , and IORDY:DDMARDY-:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

4.4.4.2 Sustained Ultra DMA data-in burst

The value for the timing for each Ultra DMA modes are contained in 4.4.4

Figure 11- Sustain Ultra DMA data-in burst



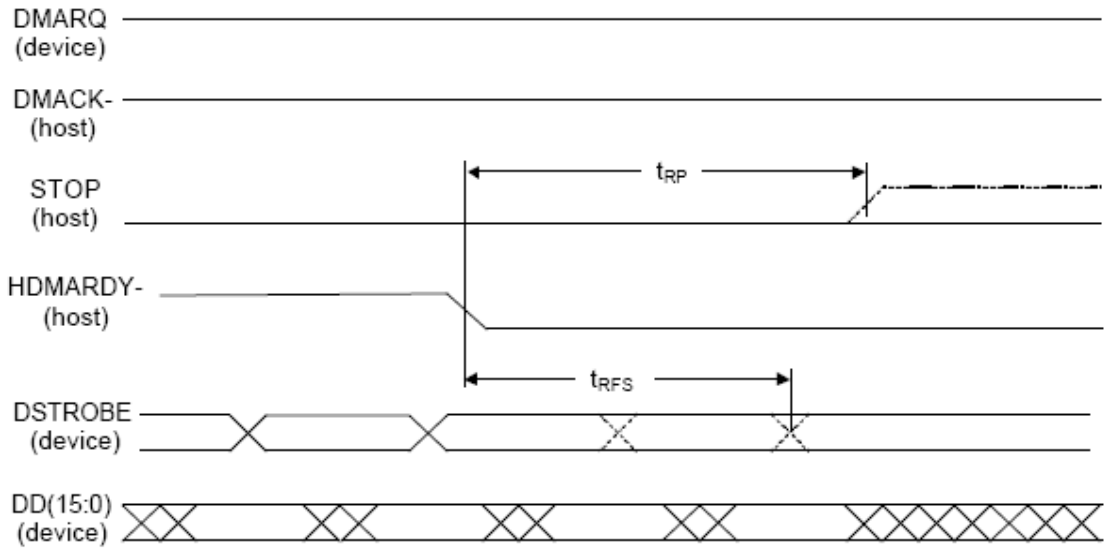
Notes-

1. DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

4.4.4.3 Host pausing an Ultra DMA data-in burst

The values for the timing for each of the Ultra DMA modes are contained in 4.4.4

Figure 12- Host pausing an Ultra DMA data-in burst



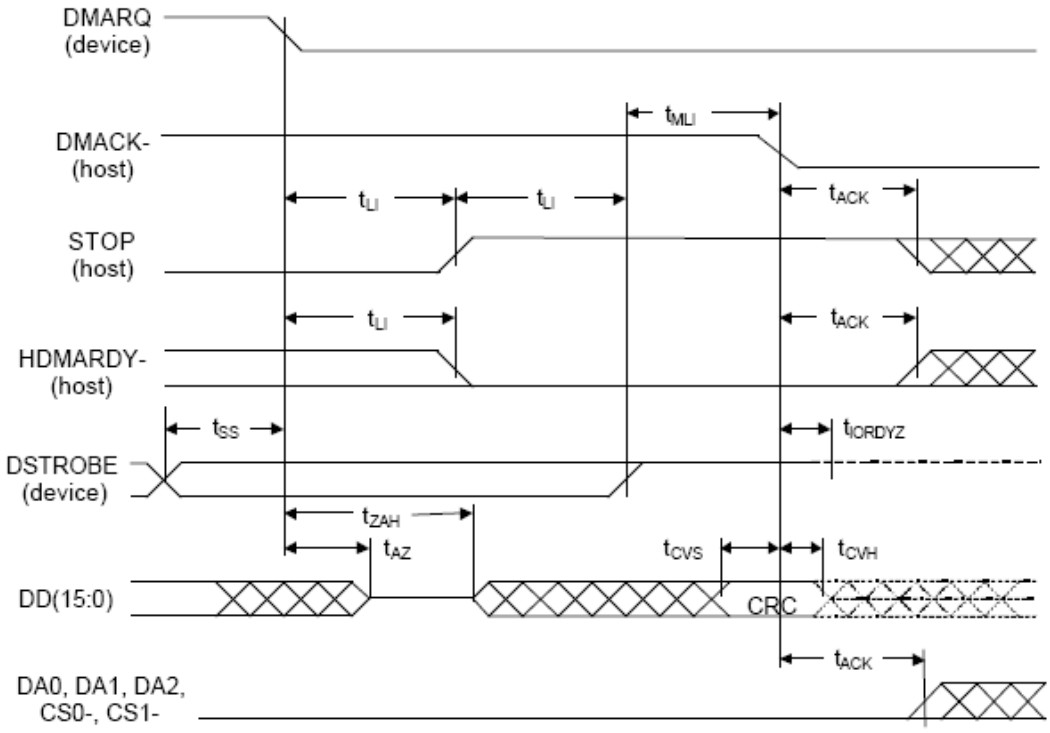
Notes-

1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than tRP after HDMARDY-, the host may receive zero, one, two, or three more data words from the device.

4.4.4.4 Device terminating an Ultra DMA data-in burst

The value for the timings for each of the Ultra DMA modes are contained in 4.4.4

Figure 13- Device terminating at Ultra DMA data-in burst



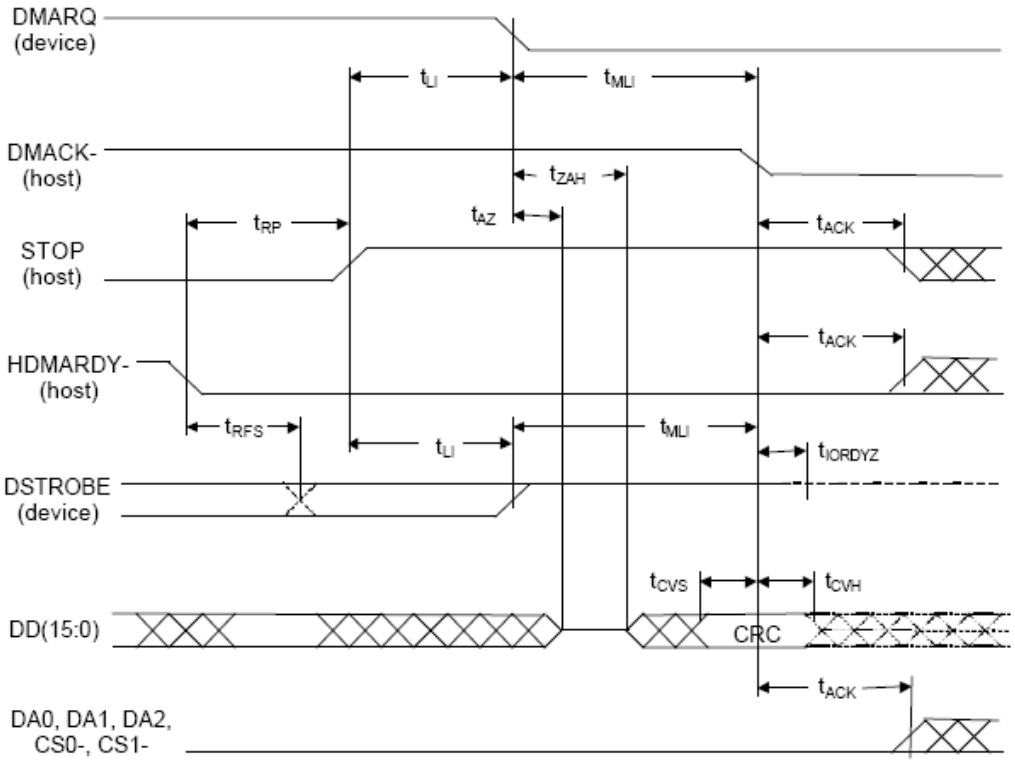
Notes-

1. *The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer effect after DMARQ and DMACK are negated.*

4.4.4.5 Host terminating an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

Figure 14- Host terminating an Ultra DMA data-in burst



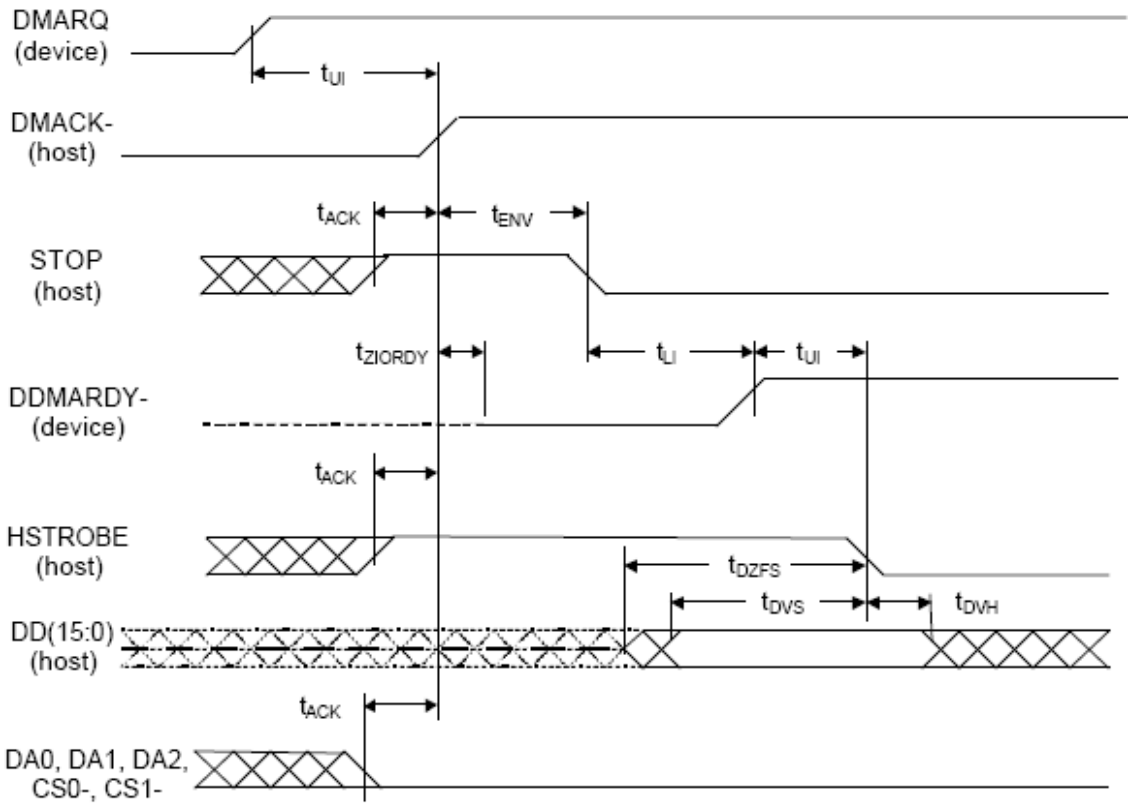
Notes-

1. *The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.*

4.4.4.6 Initiating an Ultra DMA data-out burst

The values for the timing for each the Ultra DMA modes are contained in 4.4.4

Figure 15- Initiating an Ultra DMA data-out burst



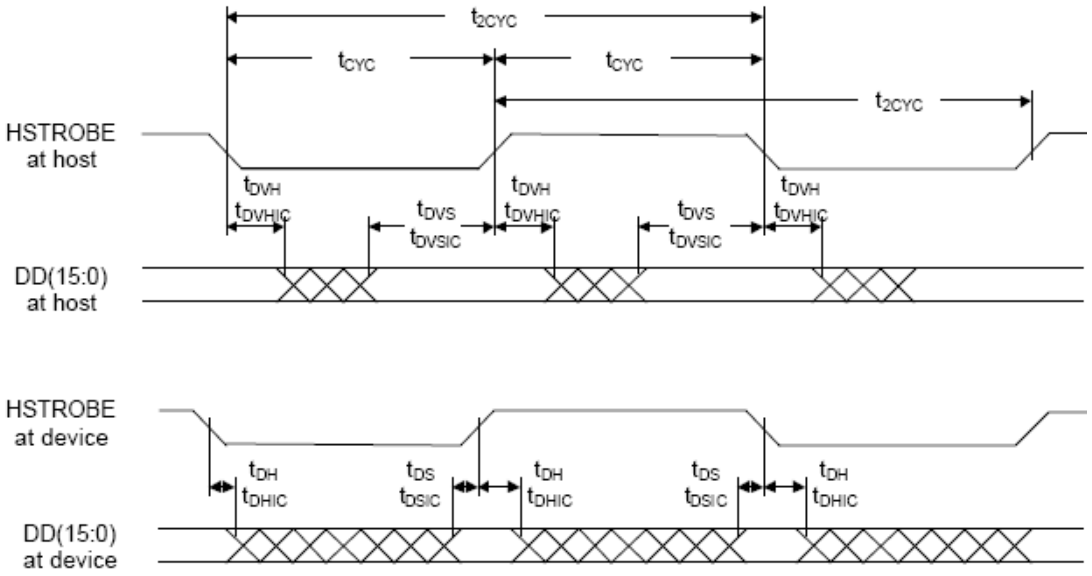
Notes-

1. *The definitions for the STOP, DDMARDY, and STROBE signal lines are not in effect until DMARQ and DMACK are asserted.*

4.4.4.7 Sustained Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

Figure 16- Sustained Ultra DMA data-out burst



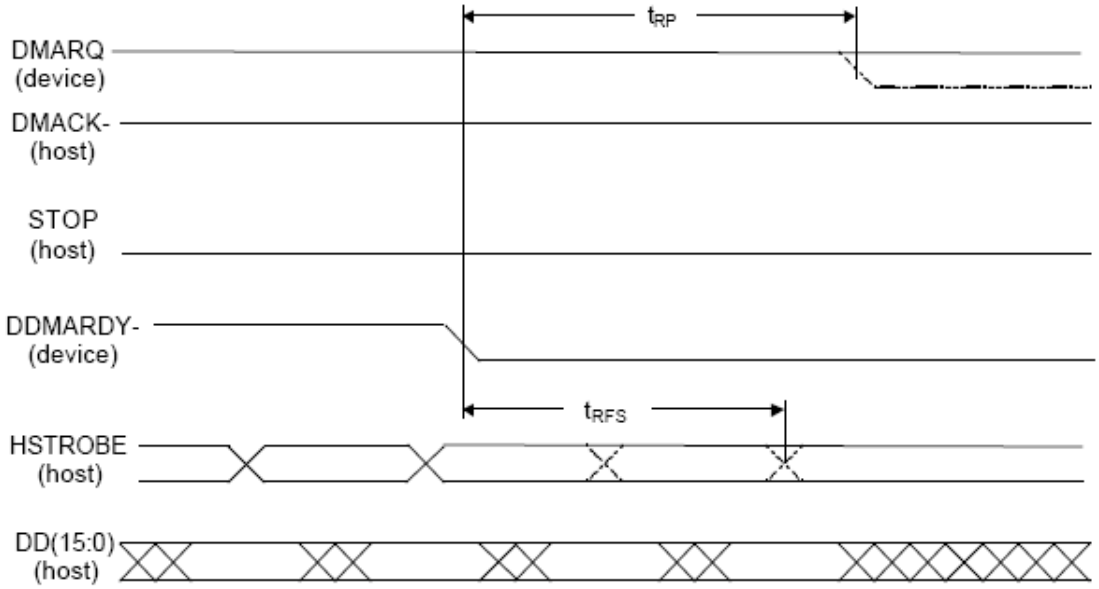
Notes-

1. *DD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.*

4.4.4.8 Device pausing an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

Figure 17- Device pausing an Ultra DMA data-out burst



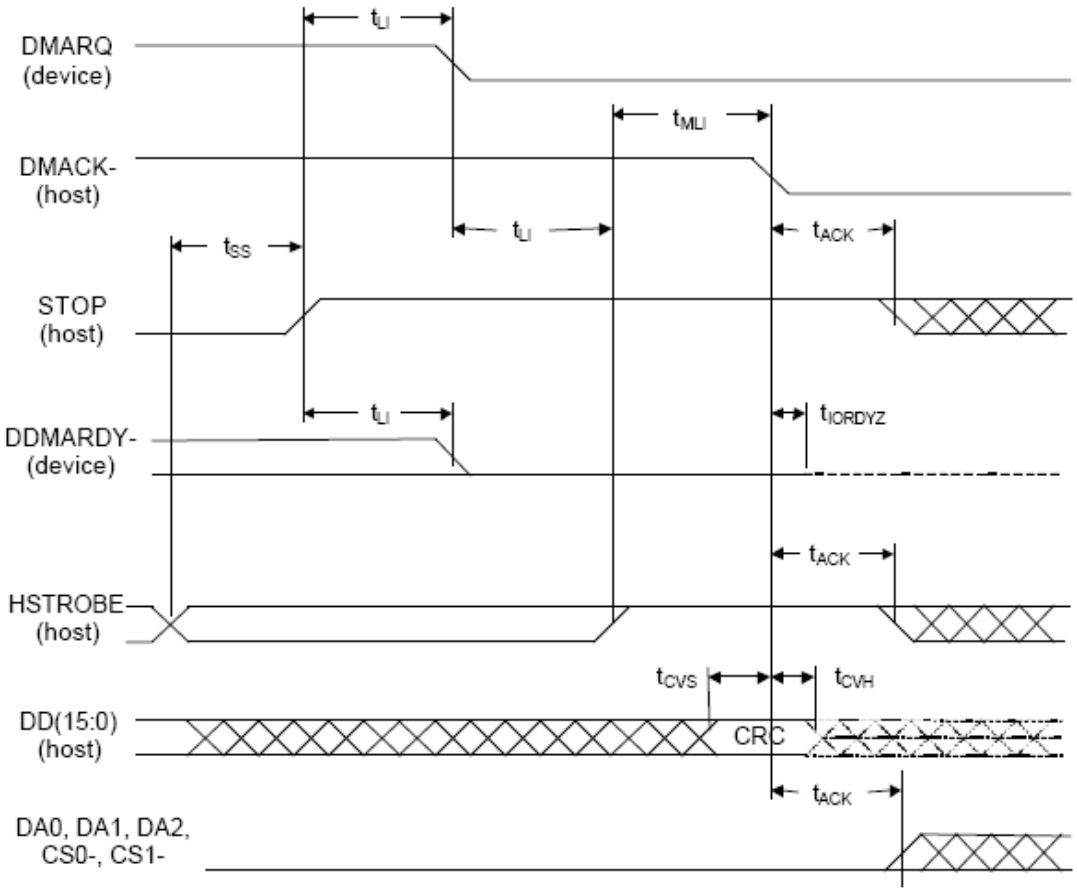
Notes-

1. The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than tRP after DDMARDY- is negated.
2. After negating DDMARDY-, the device may receive zero, one, two, or three more data words from the host.

4.4.4.9 Host terminating an Ultra DMA data-out burst

The values for timings for each of the Ultra DMA are contained in 4.4.4

Figure 18- Host terminating an Ultra DMA data-out burst



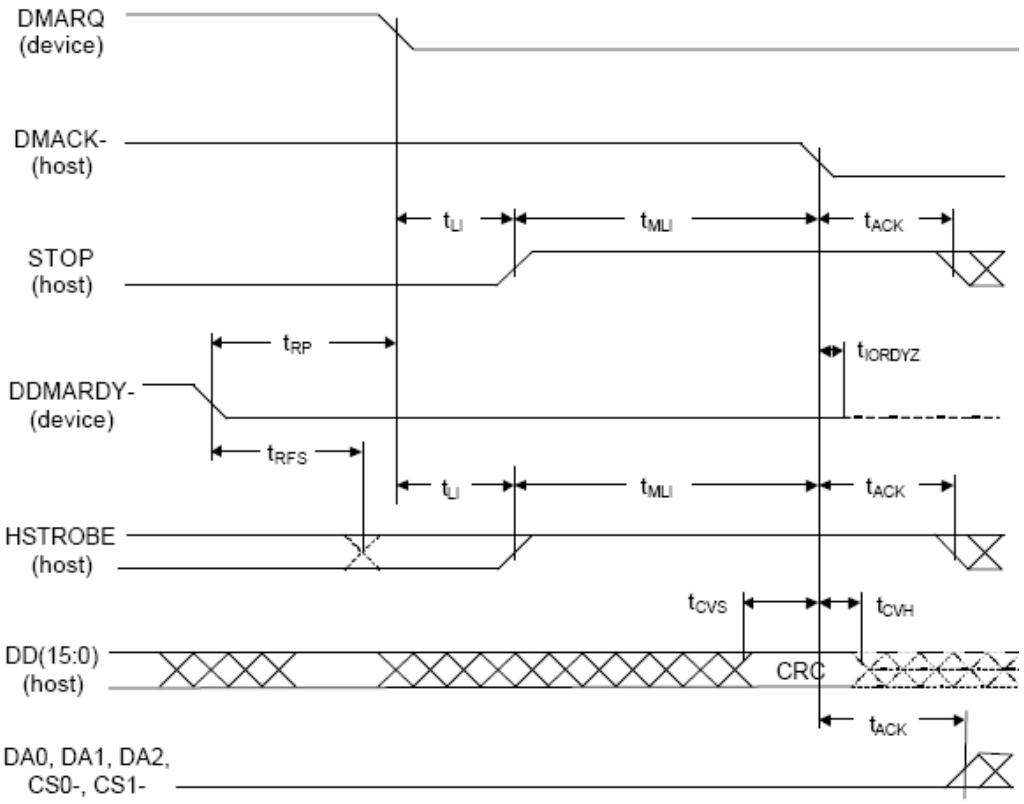
Notes-

1. The definitions for the STOP, DDMARDY, and HSTROBE signals lines are no longer in effect after DMARQ and DMACK are negated.

4.4.4.10 Device terminating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

Figure 19- Device Terminating an Ultra DMA data-out burst



Notes-

1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

5 Supported IDE Commands

FiD 2.5” ATA6000 supports the commands listed in Table11.

Table 11 IDE Commands

Command Name	Command Code	Support
Check Power Mode	E5H (98H)	Yes
Execute Device Diagnostic	90H	Yes
Format Track	(50H)	Yes
Identify Device	ECH	Yes
Idle	E3H (97H)	Yes
Idle immediate	E1H (95H)	Yes
Initialize Device Parameters	(91H)	Yes
NOP	00H	Yes
Read Buffer	E4H	Yes
Read Long Sector	(22H or 23H)	Yes
Read Multiple	C4H	Yes
Read Sector(s)	20H or 21H	Yes
Read Verify Sector	40H or 41H	Yes
Read DMA	C8H	Yes
Recalibrate	(1XH)	Yes
Seek	70H	Yes
Set Features	EFH	Yes
Set Multiple Mode	C6H	Yes
Set Sleep Mode	E6H (99H)	Yes
Standby	E2H (96H)	Yes
Standby Immediate	E0H (94H)	Yes
Write Buffer	E8H	Yes
Write Multiple	C5H	Yes
Write Sector	30H	Yes
Write DMA	CAH	Yes
Write Verify	(3CH)	Yes
Security Set Password	F1H	Yes

Security Unlock	F2H	Yes
Security Erase Prepare	F3H	Yes
Security Erase Unit	F4H	Yes
Security Freeze Lock	F5H	Yes
Security Disable Password	F6H	Yes

6 Device Parameters

FiD 2.5 ATA 6000 device parameters listed in Table 12.

Table 12 Device parameters

Capacity	LBA	Cylinders	Heads	Sectors
8GB	15988736	15861	16	63
16GB	31979776	16383	16	63
24GB	47972352	16383	16	63
32GB	63963136	16383	16	63
48GB	95944704	16383	16	63
64GB	127926272	16383	16	63
96GB	191889408	16383	16	63
128GB	255852544	16383	16	63